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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	
Filing Date	June 28, 2003
First Named Inventor	Chih-Hsin Wang
Art Unit	
Examiner Name	
Attorney Docket Number	

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Kitamura et al., "A Low Voltage Operating Flash Cell with High Coupling Ratio Using Horned Floating Gate with Fine HSE," Symposium on VLSI Technology, p.104, 1998	
		Lai, "Flash Memories: Where We Were and Where We Are Going", IEDM Technical Digest, pp.971-973, 1998,	
		Kuo et al., "TEFET - A High Density, Low Erase Voltage, Trench Flash EEPROM", Symposium on VLSI Technology, p.51, 1994	
		Wang et al, "Three-Dimensional DIBL for Shallow-Trench Isolated MOSFET's", IEEE Trans. on Electron Devices, vol. 46, pp. 139-144, 1999	

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U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,780,341	07-14-1998	Seiki Ogura	Figs. 4A, 4B, 6A, 6B
		US-			Fig. 7A
		US- 4,957,877	09-18-1990	Simon M. Tam et al.	Figs. 5A, 5B
		US- 5,146,426	09-08-1992	Mukherjee, et al	p2, c5 L17-20
		US-			c3 L46-48, c6 L45-53
		US- 5,432,739	07-11-1995	H. B. Pein	c3 L57-65
		US-			
		US- 5,115,289	05-19-1992	Hisamoto et al.	Figs. 1, 3b
		US-			c10 L66-68, c11 L44
		US-			c13 L27, c17 L14-68
		US- 6,479,863 B2	11-12-2002	John Caywood	Figs. 3b, 5b, 17d,
		US-			17e, 18d
		US- 6,372,617 B1	04-16-2002	T. Kitamura	Fig. 3A
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS

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